REMARKS

Reconsideration of the application as amended is respectfully requested. The Office Action has rejected claims 2, 6, and 8-13. Applicant has amended claims 2, 8, 9, and 10. After amendment, claims 2, 6, and 8-13 remain pending in the application. No new matter has been added by these amendments as can be confirmed by the Examiner.

Rejections under 35 U.S.C. §112

Claims 2, 6, and 8-13 stand rejected under 35 U.S.C. §112 as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. Applicant thanks the Examiner for pointing out the informalities with regard to these claims. Claims 2, 8, 9, and 10 have been amended. Applicant respectfully submits that the amended claims are allowable.

Rejections under 35 U.S.C. §102(b)

Claims 2, 6, 8, and 11 stand rejected under 35 U.S.C. §102(b) as being anticipated by U.S. Patent No. 5,896,401 to Abramovici et al ("Abramovici"). Applicant respectfully traverses the rejection.

Abramovici discloses a fault simulator for a digital combinational circuit that uses three distinct models of the digital combinational circuit – a good circuit model, a faulty circuit model, and a backward network. Col 5, lines 1-7 and Fig. 5. The Office Action focuses its attention on Abramovici's backtracing teachings. However, as will be explained, the backtracing taught by Abramovici is not the same as the backtracing required by each of the pending claims as they have been amended herein.

Applicant initially notes that in Abramovici, the backtracing is performed using both the good circuit model *and* the backward network model. The good circuit model and the backward network model disclosed in Abramovici are two different logic circuits, neither of which are are the same as the circuit to be tested. Col. 3, lines 48-54. In other words, the backtracing performed by Abramovici is *not* performed on the actual circuitry in the integrated circuit being tested.

In Abramovici, the good circuit model is a model of the circuit to be tested in a 3-valued logic system. In order to generate the good circuit model, each element of the circuit to be tested is mapped into a logic circuit that models the corresponding element in the 3-valued logic system. Thus, Abramovici discloses performing a 3-valued good machine simulation using the good circuit model *that was generated by substituting library circuit elements for actual circuits found on the integrated circuit being tested.* As Abramovici teaches, each signal of the circuit to be tested is represented by two bits in the 3-valued logic system. Col. 5, lines 9-11.[1]

In Abramovici, backtracing is performed using a backward network *model* that receives the results of the 3-valued logic simulation performed on the good circuit *model*, which determines the critical nodes of the circuit to be tested. The backward network *model* has one primary input for every output of the circuit to be tested and one primary output for every input of the circuit to be tested. The backward network *model* is a logic circuit that calculates the criticality values for inputs of every logic gate in the circuit to be tested, where the outputs of the logic gate are critical. Col. 5, lines 39-52, and Fig. 9. The backward network model is *not* the integrated circuit that will be tested.

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[1] In the 3-valued logic system, each signal A is represented using two bits A0 and A1. When A0 is 1, A has the value "0" or "x." When A1 is 1, A has the value "1" or "x." Finally, when A0 and A1 are both 1, A has the unknown value "x." Col. 5, lines 11-27 and Fig. 6(a-c).

Unlike each of the independent claims 2 and 8 as they have been amended, Abramovici does not teach " performing a good machine simulation on the IC with the test to obtain values of each internal node of the IC." As discussed above, Abramovici performs a 3-valued good machine simulation using a good circuit model of the circuit to be tested. Unlike what is required by the claims, the good circuit model is *not* the integrated circuit that is being tested. Instead, as discussed, the good circuit model is a logic circuit that is separate and distinct from the circuit to be tested. Therefore, Abramovici does not disclose performing a good machine simulation *on the IC*, as required by claims 2 and 8. Moreover, as discussed above, in the good circuit model disclosed in Abramovici, each signal of the circuit to be tested is represented using two bits in the 3-valued logic system. The good machine simulation of Abramovici generates the two bit values for each signal as represented in the 3-valued logic system. Applicant respectfully submits that the two bit values for each signal obtained from the circuit to be tested are not the *values of each internal node of the IC*, which is required by claims 2 and 8.

Thus, unlike each of the amended independent claims 2 and 8, Abramovici does not teach "backtracing, in a single detection pass, through logic gates and memory elements of the IC, starting at each observable node," where the backtracing is "based on outputs of said logic gates and memory elements," and where the outputs are "obtained from said good machine simulation." In fact, as discussed, the good circuit model, and the backward network disclosed in Abramovici are combinational circuits *distinct from the logic gates of the IC*. Figs. 6(b), 6(c), 9 and accompanying text. Moreover, as discussed, the good circuit model in Abramovici is a model that performs 3-valued logic simulation. As discussed above, the 3-valued logic simulation is performed using a combinational circuit that is not the same as the logic gates of the IC. Therefore, the good machine simulation in Abarmovici is not performed on the IC, and

the backtracing in Abramovici is not based on "outputs of said logic gates and memory elements" of the IC. Abramovici also does not teach "backtracing, in a single detection pass, through logic gates and memory elements of the IC" because the backward network used to determine critical nodes in Abramovici is not the same as the logic gates of the IC.

Finally, Applicant notes that Abramovici does not disclose backtracing in a single detection pass *through memory elements*. Abramovici only discloses generation of the good circuit model and the backward network model for AND gates, OR gates, and inverters. Col. 5, line 53 - Col. 6, line 12 and Fig. 9. Applicant respectfully submits that Abramovici contains no teachings relating to backtracing through memory elements. That this is the case is demonstrated by the fact that the Office Action made no attempt to show where Abramovici discloses such a feature.

Based on the forgoing, Applicant respectfully submits that claims 2 and 8 are allowable over Abramovici. Because claim 6 depends from claim 2 and claim 11 is dependent on claim 8, Applicant respectfully submits that they are allowable as well.

Rejections Under 35 U.S.C. §103

Claims 9, 10, 12, and 13 stand rejected under 35 U.S.C. §103 as being unpatentable over Abramovici. Applicant respectfully traverses the rejection. In accordance with M.P.E.P. § 2142, the Examiner bears the initial burden of establishing a *prima facie* case of obviousness. "To establish a *prima facie* case of obviousness, three basic criteria must be met." (M.P.E.P. § 2143.) First, some suggestion or motivation in the prior art references or in the knowledge of one of ordinary skill in the relevant art must exist to modify or combine the references. Second, if the references are combined, a reasonable expectation of success must be shown. Then, finally, all

of the claim limitations must be taught or suggested by one reference or a combination of references. To establish a *prima facie* case of obviousness based on a single reference that does not teach all the elements of a claim, the Examiner must provide a rationale for modifying the teachings of the reference. See *In re Kotzab*, 55 U.S.P.Q.2d 1313, 1317 (Fed. Cir. 2000), *citing*, *B.F. Goodrich Co. v. Aircraft Breaking Sys. Corp.*, 72 F.3d 1577, 1582, 37 U.S.P.Q.2d 1314, 1318 (Fed. Cir. 1996).

Claims 9 and 10 contain the same limitations discussed above with respect to claims 2 and 8. As discussed above, Abramovici is missing limitations required by claims 9 and 10. In fact, as seen above, Abramovici is fundamentally different than the system required by the present claims. Because Abramovici fails to teach or suggest any of the limitations discussed above, Applicant respectfully submits that Abramovici cannot render these claims obvious.

Based on the forgoing, Applicant respectfully submits that claims 9 and 10 are allowable over Abramovici. Because claim 12 depends from claim 9 and claim 13 is dependent on claim 10, Applicant respectfully submits that they are allowable as well.

Applicant would also like to note that the Attorney Docket No. was changed when the current attorney took over prosecution of this matter. Applicant requests that the Patent Office change their records to reflect this new reference number which is 700693-4011.

Conclusion

In view of the foregoing, Applicant respectfully submits that this application is in condition for allowance, which is respectfully requested. A Notice of Allowance is earnestly solicited at the earliest possible date. If the Examiner believes that a telephone conference would be useful in moving the application forward to allowance, the Examiner is encouraged to contact

the undersigned at (650) 614-7669. If there are any additional fees required, please charge Deposit Account No. 15-0665.

Respectfully submitted,

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